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A Study of Five-Level FCMLI Based STATCOM

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Abstract: This paper deals with the study and analysis of various types of multi level inverter among which the five level Flying Capacitor Multi Level Inverter (FCMLI) based on compensating devices like STATCOM has been analyzed in detail and the waveforms are studied. This inverter is used for power oscillation damping and voltage control of power system. In this paper various switching sequences and modulation index has been studied.

Keywords: *FCMLI, Statcom, Multilevel Inverter, Modulation index.*

1. INTRODUCTION:

The multilevel inverter was first introduced in 1975. The three level converters was the first multilevel inverter introduced. A multilevel converter is a power electronic system that synthesizes a desired output voltage from several levels of dc voltages as inputs. With an increasing number of dc voltage sources, the converter output voltage waveform approaches a nearly sinusoidal waveform while using a fundamental frequency-switching scheme. The primary advantage of multilevel inverter is their small output voltage, results in higher output quality, lower harmonic component, better electromagnetic computability, and lower switching losses.

2. TYPES OF MULTILEVEL INVERTERS

The general structure of the multilevel converter is to synthesize a near sinusoidal voltage from several levels of dc voltages, typically obtained from the capacitor voltage sources. As the number of levels increases, the synthesized output waveform has more steps, which produce a staircase wave that approaches a desired waveform. Also, as more steps are added to the waveform, the harmonic distortion of the output wave decreases, approaching zero as the number of levels increases. As the number of levels increases, the voltage that can be spanned by summing multiple voltage levels also increases.

The multilevel inverters can be classified into three types

1. Diode-clamped multilevel inverter;
2. Flying-capacitors multilevel inverter;
3. Cascade multilevel inverter.

3 FLYING CAPACITORS MULTILEVEL INVERTER (FCMLI)

Fig 1 shows a typical configuration of a five-level flying-capacitor inverter. It is evolved from the two-level inverter by adding dc capacitors to the cascaded switches. There are four complementary switch pairs in each of the inverter legs. For example, the switch pairs in leg *A*are (S_1, S'_1), (S_2,S'_2), (S_3,S'_3) and (S_4, S'_4). Therefore, only four independent gate signals are required for each inverter phase. The flying-capacitor inverter can produce an inverter phase voltage with five voltage levels. When switches S_1 , S_2 , S_3 and S_4 conduct, the inverter phase voltage v_{AN} is 4*E*, which is the voltage at the inverter terminal *A* with respect to the negative dc bus *N*.

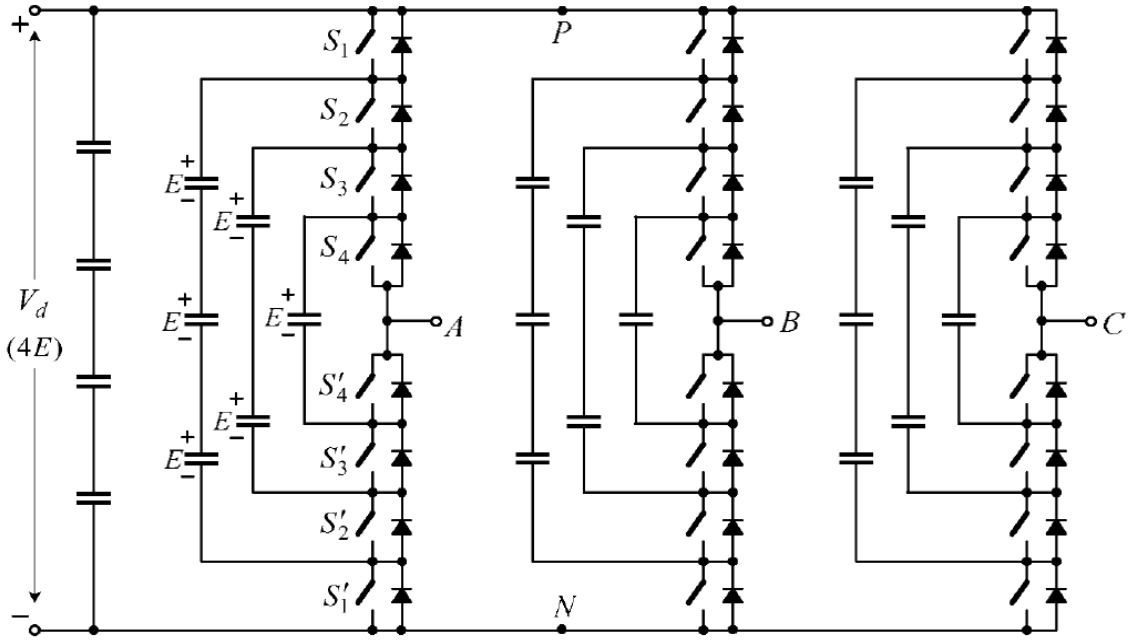


Fig 1: configuration of a five-level flying-capacitor inverter

Similarly, with S_1, S_2, and S_3 switched on, v_{AN}. It is noted that some voltage levels can be obtained by more than one switching state. The voltage level 2*E*, for instance, can be produced by six sets of different switching states. The switching state redundancy is a common phenomenon in multilevel converters, which provides a great flexibility for the switching pattern design.

3.1 Modulation Schemes

Both phase- and level-shifted modulation schemes can be implemented for the multilevel flying-capacitor inverters.Since the flying-capacitor inverter topology is derived from the two-level inverter, it carries the same features as the two-level inverter such as modular structure for the switching devices. It is also a multilevel inverter, producing the voltage waveforms with reduced *dv/dt*and THD. However, the flying-capacitor inverter has some limitations, including the following:

1. A large number of dc capacitors with separate pre-charge circuits. The inverter requires several banks of bulky dc capacitors, each of which needs a separate pre-charge circuit.
2. Complex capacitor voltage balancing control. The dc capacitor voltages in the inverter normally vary with the inverter operating conditions. To avoid the problems caused by the dc voltage deviation, the voltages on the dc flying capacitors should be tightly controlled, which increases the complexity of the control scheme.
3. Due to the above-mentioned drawbacks, the practical use of the flying-capacitor inverter in the drive system seems limited.

4. FCMLI BASED STATCOM

This section describes the use of the STATCOM based on the five-level flying capacitor inverter for power oscillation damping and voltage control of power system. The study is based on an SMIB system with the STATCOM connected in Shunt at the midpoint of the transmission line

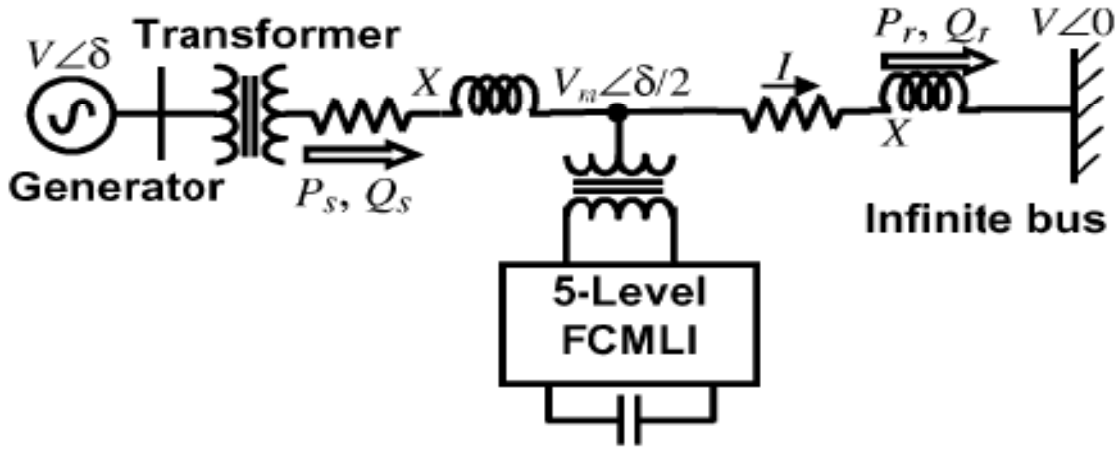


Fig. 2 Block diagram of five-level FCMLI based STATCOM

A STATCOM is a device that can provide reactive power support to a bus. It is useful in improving the transient stability, power oscillation damping, voltage stability, and increase in power transfer limit of the connected power system. It consists of a voltage source inverter connected to an energy storage device on one side and to the power system on the other side. A STATCOM can be viewed as a controllable ac voltage source, which appears behind a transformer leakage reactance. The active and reactive power transfer is caused by the voltage difference across this reactance. Usually, the inverter output voltage is almost in phase with the voltage of the ac system. Therefore, only reactive power transfer occurs, whose quantity and sign depend on the magnitude of the inverter output voltage vis-à-vis that of midpoint ac voltage. If it is higher than ac voltage the
reactive power is supplied to the system and if it is lower the converter circuit absorbs the reactive power. The magnitude of the inverter output voltage depends on the modulation index and the dc-link voltage.

4.1STATCOM control scheme

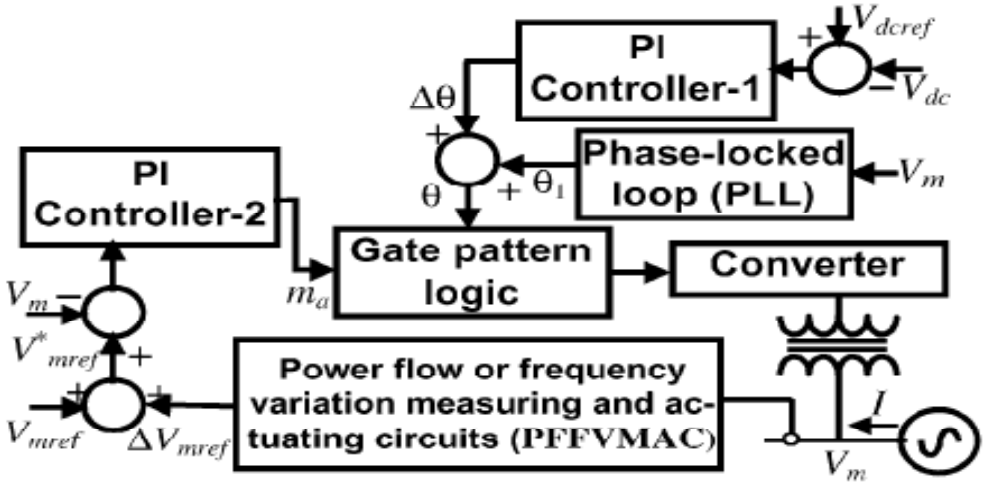


Fig.3 Block diagram of the STATCOM control scheme

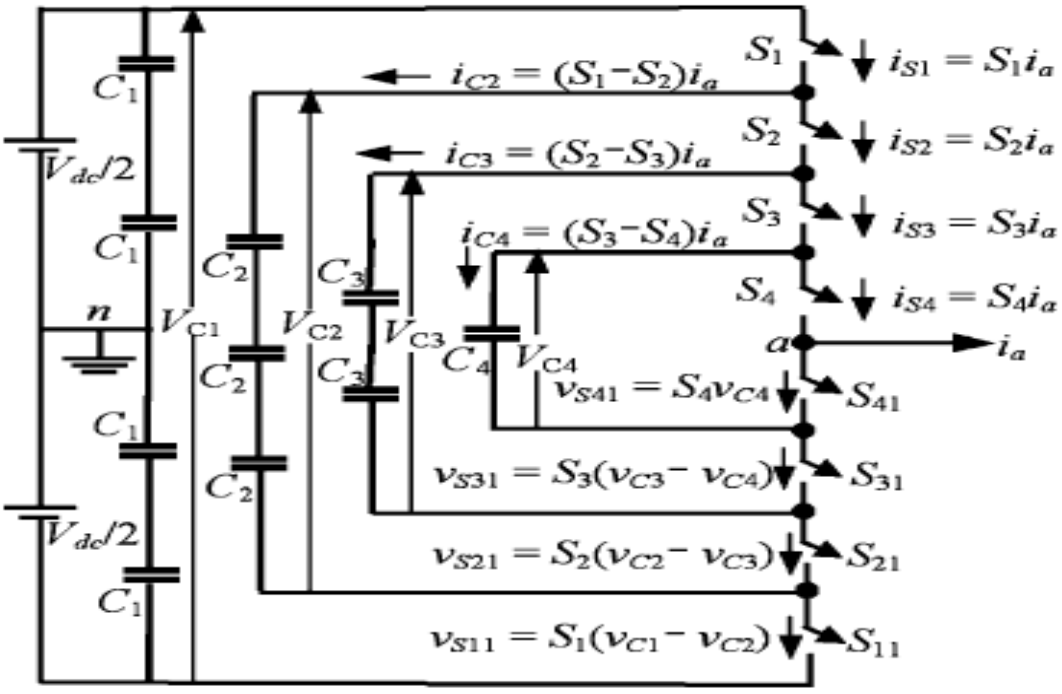
There are many strategies to control the operation of STATCOM such as PI control, pole placement control and linear quadratic controlThe PI control scheme has been used here to study the performance of the system.

In normal operation, for the voltage control of a bus, the value of Vm_{ref} depends on the desired voltage profile at that particular bus; therefore, the power flow or frequency variation measuring and actuating circuits (PFFVMAC) are not needed. The PFFVMAC block is needed when some feedback signal is taken from the power system for improving the transient stability of the system. There are twoControl objectives in the STATCOM control: ac-bus voltage control and dc-link voltage control. Therefore, two internal control loops containing two PI controllers are used here. The dc capacitor voltage is regulated around a reference value Vdc_{ref}which is kept fixed and is chosen considering the rating of the STATCOM. Since the output voltage of the inverter and V_m should be in phase, a phase-locked loop (PLL) is used that has V_m as input and angle Q_1 as output. Ideally, for pure reactive power exchange between the compensator and the line, the dc link voltage should remain constant. However, the capacitor discharges due to losses in switching, snubber circuits, and in transformers. Therefore, to keep the capacitor voltage constant, some amount of real power exchange is needed between the inverter and the ac system.

The PI controller-1, with an input of the error between V_{dc}ref and $V_{dc}$and output Δ_Q facilitates this power exchange. If the inverter output voltage is made to lag the voltage of the ac system then the active power flow is from the ac system to the dc side of the inverter charging the capacitor. The reverse will happen when the corresponding phase relation is reversed. Another control loop (PI contoller-2) generates the modulation index.

The input to this PI controller is the difference between the reference rms value V_{mref} and the actual rms value of the voltage V_m at the point of connection. Therefore, in the control system shown in Fig.4.2, one loop sets the angle of the injected voltage to regulate the dc capacitor voltage while the other loop sets the modulation index to generate the required voltage profile.

4.2 Basic Configuration of a Five-Level Flying Capacitor Inverter



One phase leg of a five-level Flying capacitor inverter.

Fig.4. configuration of per phase diagram

Fig.4 shows one phase of a five-level flying capacitor inverter. In the figure each switch $s_1$tos$_4$ and s_{11}tos$_{41}$ consists of a power semiconductor switch and an anti parallel diode. The pairs of the switches (s_1, s_{41}), (s_2, s_{21}), (s_3, s_{31}), and (s_4, s_{41}) are closed in complementary manner. Thus, if s_1 is ON, s_{11} is OFF and vice-versa. Each capacitor shown in the figure is of equal voltage rating. Let us consider the group of capacitors in a single clamping leg as one equivalent capacitor and call them C_1, C_2, C_3, and C_4. Then C_1, is the main dc-link capacitor, this is required to be regulated externally. Therefore, either a battery of suitable rating is connected in place of C_1 (or) C_1 without the battery connected across it is regulated around a reference dc-link voltage using the real power exchange from the line. For a three-phase inverter two more phases of the same construction are coupled to the same dc-link. C_2, C_3, and C_4 are flying capacitors that provide the multilevel voltage ability to the converter. The flying capacitors of one phase are independent from those of other phases. If the voltage V_{C1} is V_{dc}, then V_{c2}, V_{c3}, and V_{c4} are $3V_{dc}$ / 4, $V_{dc}/2$, and $V_{dc}/4$, respectively. For any initial state of clamping voltages the inverter output voltage is given by

$$V_{an} = S_1(V_{C1} - V_{C2}) + S_2(V_{C2} - V_{C3}) + S_3(V_{C3} - V_{C4}) + S_4V_{C4} - V_{C1}/2. \quad \text{------- (1)}$$

4.3 Switching Scheme for a Five-Level FCMLI

Table1 switching scheme

S_1	S_2	S_3	S_4	C_2	C_3	C_4	V_{an}
ON	ON	ON	ON	NC	NC	NC	$+V_{dc}/2$
ON	ON	ON	OFF	NC	NC	+	$+V_{dc}/4$
ON	ON	OFF	ON	NC	+	–	
ON	OFF	ON	ON	+	–	NC	
OFF	ON	ON	ON	–	NC	NC	
OFF	OFF	ON	ON	NC	–	NC	0
OFF	ON	OFF	ON	–	+	–	
OFF	ON	ON	OFF	–	NC	+	
ON	OFF	OFF	ON	+	NC	–	
ON	OFF	ON	OFF	+	–	+	
ON	ON	OFF	OFF	NC	+	NC	
ON	OFF	OFF	OFF	+	NC	NC	$-V_{dc}/4$
OFF	ON	OFF	OFF	–	+	NC	
OFF	OFF	ON	OFF	NC	–	+	
OFF	OFF	OFF	ON	NC	NC	–	
OFF	OFF	OFF	OFF	NC	NC	NC	$-V_{dc}/2$

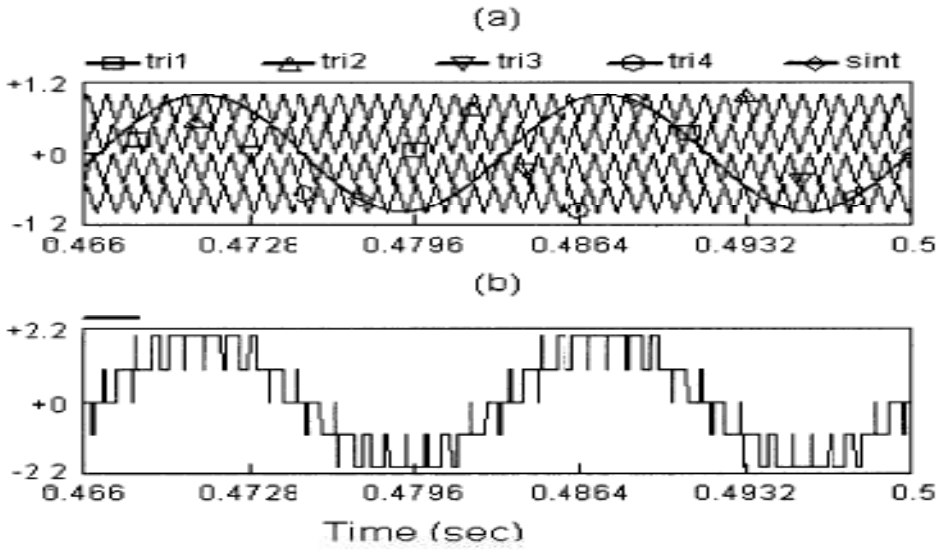
InTable and in (1), the switching states S_1toS_4 take the value 1 if the corresponding switch is conducting and 0 otherwise. Based on (1), the switch combinations given in Table I are used to synthesize the output voltage V_{an} of phase-a with respect to the neutral point n. Table I also indicates the states of the flying capacitors corresponding to the switching combinations chosen. The neither state NC indicates that the capacitor neither charges nor discharges in this mode. The states +and - denote the charging and discharging respectively of the corresponding capacitors. The capacitor states (+and -) will reverse for the negative half cycle of the current The output voltage for an n-level inverter can similarly be defined. In general, an n-level FCMLI requires(n-1)pairs of power semiconductor devices and (n-1)*(n-2)/2clamping capacitors per phase leg in addition to(n-1) main dc bus capacitors provided all the capacitors are of equal value. The number of capacitors can be reduced by sizing the capacitors in a single leg as an equivalent one.

The size of the voltage increment between two consecutive clamping legs defines the size of voltage steps in the output waveform. The voltage of the innermost clamping leg (e.g.,C_4in Fig. 4) clamping the innermost two devices is $V_{dc}/(n-1)$.

The voltage of the next innermost clamping leg will be $V_{dc}/(n-1)+ V_{dc}/(n-1) =2V_{dc} /(n-1)$ and so on. Thus, each next clamping leg will have the voltage increment of $V_{dc}/(n-1)$ from its immediate inner one. The voltage stress across each capacitor is $V_{dc}/(n-1)$.The voltage levels and the arrangements of the flying capacitors in the FCMLI structure assure that the voltage stress across each main device is same and is equal to $V_{dc}/(n-1)$.

The line-to-line output voltage of the inverter varies from $+V_{dc}$ to- V_{dc} and has (2n-1) levels in the output, while the phase voltage varies from $+V_{dc}$ to- V_{dc} with n-levels. It can be seen from Table I that the structure offers multiple switching combinations for $V_{an=}V_{dc}/4$,0 and- $V_{dc}/4$. Since such redundancies are available, one can choose a preferential switching state that will help in maintaining the capacitor voltages constant. However, the switching combination chosen affects the current rating of the capacitors.

4.4 Modulation Scheme



Modulation scheme. (a) SPWM. (b) Output waveform.

Fig.5Modulation scheme

There are the various strategies developed to improve the output voltage and reduce the harmonics, sinusoidal pulse width modulation (SPWM) strategy is employed here. In this method for an n-level inverter, (n-1) carrier waves are compared with a controlled sinusoidal modulating signal and the switching rules for the switches are decided by their intersections. The output signal of the comparator resembles with the output voltage waveform of the inverter and decides the voltage level that must be generated at a particular instant. For a five-level inverter, a modulating signal and 4 carrier waves are required for each phase of the inverter as shown in Fig. 3.4. The modulating signals of each phase are displaced from each other by 120 degree. The phase shift angle of the modulating signal, i.e. ɵ, depends on the application requirements, The modulation index m_a is given by

$$m_a = A_m/2A_c$$

where $A_m$is the amplitude of the modulating signal and A_c is that of one carrier wave (peak to peak). Here, the carrier waves are taken to have phase displacement of 120 for smallest distortion in the output and their frequency is taken as n_c times to that of the modulating signal, where n_c is a multiple of three so that triplen harmonic cancellation takes place across the three-phase inverter load . The carrier waves and the modulating signals are compared and the output of the comparator defines the output voltage waveform. It is assumed that the modulating signal varies from +0.98to -0.98. The amplitudes of the four carrier waves are from 0 to 0.5, 0.5 to 1, in the positive half cycle of the modulating signal, and from 0 to to-0.5, -0.5 to -1, in the negative half cycle. The modulating signal and four carrier waves are compared in four comparators, on instantaneous basis. The comparator output is +1when the

modulating signal exceeds the carrier wave and zero otherwise.

4.5 Phase Locked Loop

PLL stands for 'Phase-Locked Loop' and is basically a closed loop frequency control system, which functioning is based on the phase sensitive detection of phase difference between the input and output signals of the controlled oscillator (CO). The Phase Locked Loop method of frequency synthesis is now the most commonly used method of producing high frequency oscillations in modern communications equipment. Phase locked loop systems to generate stable high frequency oscillations.

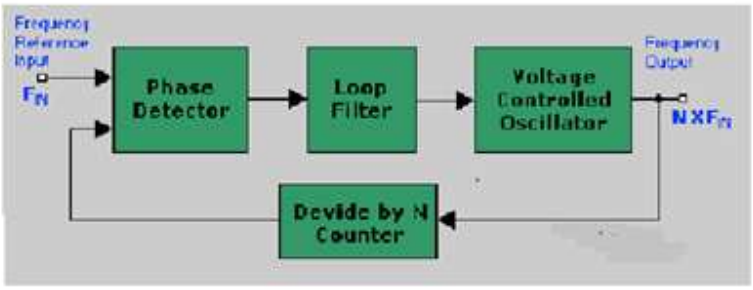


Fig 6 phase locked loop

Fig 6 shows the classic configuration phase locked loop. The phase detector is a device that compares two input frequencies, generating an output that is a measure of their phase difference (if, for example, they differ in frequency, it gives a periodic output at the difference frequency). If f_{IN}doesn't equal f_{VCO}, the phase-error signal, after being filtered and amplified, causes the VCO frequency to deviate in the direction of f_{IN}. If conditions are right, the VCO will quickly "lock" to f_{IN} maintaining a fixed relationship with the input signal.

At that point the filtered output of the phase detector is a dc signal, and the control input to the VCO is a measure of the input frequency, with obvious applications to tone decoding (used in digital transmission over telephone lines) and FM detection. The VCO output is a locally generated frequency equal to f_{IN}, thus providing a clean replica of f_{IN}, which may itself be noisy. Since the VCO output can be a triangle wave, sine wave, or whatever, this provides a nice method of generating a sine wave, say, locked to a train of pulses. In one of the most common applications of PLLs, a modulo-*n* counter is hooked between the VCO output and the phase detector, thus generating a multiple of the input reference frequency f_{IN}. This is an ideal method for generating clocking pulses at a multiple of the power-line frequency for integrating A/D converters (dual-slope, charge-balancing), in order to have infinite rejection of interference at the power-line frequency and its harmonics. It also provides the basic technique of frequency synthesizers.

5. CONCLUSION:

Thus the various types of multilevel inverter have been studied and also the working of five level inverter has been analyzed. It is found that as more steps are added to the waveform, the harmonic distortion of the output waveform decreases, approaching zero as the number of levels increases. The THD value has been compared for all the four topologies. From that comparison, it can be seen that the eleven level inverter has the least value of THD.

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